

**ABSTRACT:****A PARALLEL COUNTER AND A MULTIPLICATION LOGIC CIRCUIT**

A parallel counter comprises logic for generating output bits as symmetrical functions of the input bits. The parallel counter can be used in a multiplication circuit. A multiplication circuit is also provided in which an array of combinations of each bit of a binary number with each other bit of another binary number is generated having a reduced form in order to reduce the steps required in array reduction.

105210-15669460

"Express Mail" mailing label number: EL618477517US

Date of Deposit: January 25, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

---